WHAT IS CLAIMED IS:

1. A multi-finger transistor, comprising

a plurality of parallel transistors, wherein each transistor comprises:

a gate dielectric layer and a gate on a substrate;

a source/drain region in the substrate beside the gate; and

a drift region in the peripheral substrate of the source/drain region separating the source/drain region and a channel region under the gate, wherein

a width of the drift region extending from a side boundary of the source/drain region increases stepwise from edge sections of the multi-finger transistor toward a central section of the multi-finger transistor.

2. The multi-finger transistor of claim 1, wherein the multi-finger transistor is divided into $2m+1$ sections along an arrangement direction of the parallel transistors, wherein $m$ is a positive integer, and the drift region extension width is smallest in the outmost sections and increases toward the central section of the multi-finger transistor.

3. The multi-finger transistor of claim 2, wherein $m$ is 1 or 2.

4. The multi-finger transistor of claim 2, wherein the drift region extension width is zero in the outmost sections.

5. The multi-finger transistor of claim 1, wherein the drift region of a transistor is located under an isolation layer, and the gate of the same transistor partially covers the isolation layer.

6. The multi-finger transistor of claim 5, wherein the isolation layer comprises a field oxide layer.

7. The multi-finger transistor of claim 1, wherein two adjacent transistors share a source region or a drain region.

8. The multi-finger transistor of claim 7, wherein a width of the drain region is larger than a width of the source region.

9. A multi-finger transistor, comprising

a plurality of parallel transistors, wherein each transistor comprises:

a gate dielectric layer and a gate on a substrate, wherein the substrate further has a pick-up region thereon;

a source/drain region in the substrate beside the gate; and

a drift region in the peripheral substrate of the source/drain region separating the source/drain region and a channel region under the gate, wherein

a width of the drift region extending from a side boundary of the source/drain region increases with an increase in a distance between the transistor and the pick-up region.

10. The multi-finger transistor of claim 9, wherein the drift region of a transistor is located under an isolation layer, and the gate of the same transistor partially covers the isolation layer.

11. The multi-finger transistor of claim 10, wherein the isolation layer comprises a field oxide layer.

12. The multi-finger transistor of claim 9, wherein two adjacent transistors share a source region or a drain region.

13. The multi-finger transistor of claim 12, wherein a width of the drain region is larger than a width of the source region.